

What is claimed is:

- 1 1. A method comprising:
2 supplying a negative voltage to at least one
3 deselected wordline of a memory array.

- 1 2. The method of claim 1, further comprising
2 supplying a positive voltage to a selected wordline of the
3 memory array to program the selected wordline while
4 supplying the negative voltage.

- 1 3. The method of claim 2, further comprising
2 supplying the negative voltage to all wordlines of the
3 memory array except the selected wordline.

- 1 4. The method of claim 2, further comprising
2 providing a second positive voltage signal to a selected
3 bitline of the memory array.

- 1 5. The method of claim 4, further comprising
2 reducing a leakage current through at least one deselected
3 cell coupled to the selected bitline of the memory array.

- 1 6. The method of claim 1, further comprising
2 providing the negative voltage and a control negative
3 voltage to a decoder coupled to the at least one deselected
4 wordline.

1 7. The method of claim 6, further comprising
2 providing the control negative voltage to a substrate of a
3 transistor of the decoder.

1 8. The method of claim 1, further comprising
2 supplying the negative voltage at less than or equal to
3 negative one volt.

1 9. The method of claim 1, further comprising
2 supplying the negative voltage to the deselected wordline
3 during a first time period, and supplying a positive
4 voltage to the same wordline during a second time period to
5 program memory cells coupled thereto.

1 10. An apparatus comprising:
2 a decoder to supply a negative voltage to a deselected
3 address line of a memory array.

1 11. The apparatus of claim 10, wherein the decoder is
2 further coupled to supply a positive voltage to the same
3 address line if it is selected to be programmed.

1 12. The apparatus of claim 10, wherein the decoder
2 comprises a first transistor having a well coupled to
3 receive a negative control voltage, a source terminal

4 coupled to receive the negative voltage, and a drain
5 terminal coupled to pass the negative voltage to the
6 deselected address line.

1 13. The apparatus of claim 12, further comprising a
2 second transistor coupled to the first transistor and the
3 deselected address line to pass a program pulse to the
4 deselected address line if it becomes a selected address
5 line.

1 14. The apparatus of claim 12, further comprising a
2 pre-driver circuit to disable the first transistor if the
3 deselected address line becomes a selected address line.

1 15. The apparatus of claim 10, further comprising a
2 plurality of memory cells coupled to the decoder via the
3 deselected address line.

1 16. The apparatus of claim 15, wherein the plurality
2 of memory cells comprise multi-level cells of a flash
3 memory.

1 17. An article comprising a machine-readable storage
2 medium containing instructions that if executed enable a
3 system to:

4 supply a negative voltage to at least one deselected
5 wordline of a memory array.

1 18. The article of claim 17, further comprising
2 instructions that if executed enable the system to supply a
3 positive voltage to a selected wordline of the memory array
4 to program the selected wordline while the negative voltage
5 is supplied to the at least one deselected wordline.

1 19. The article of claim 18, further comprising
2 instructions that if executed enable the system to supply
3 the negative voltage to all wordlines of the memory array
4 except the selected wordline.

1 20. The article of claim 17, further comprising
2 instructions that if executed enable the system to provide
3 a negative control voltage to a substrate of a transistor
4 coupled to pass the negative voltage to the at least one
5 deselected wordline.

1 21. The article of claim 17, further comprising
2 instructions that if executed enable the system to supply
3 the negative voltage at less than or equal to negative one
4 volt.

1 22. A system comprising:

2 a memory array having a plurality of memory cells each
3 coupled to wordline and a bitline;
4 a decoder coupled to the memory array to supply a
5 negative voltage to a deselected wordline of the memory
6 array; and
7 a wireless interface coupled to the memory array.

1 23. The system of claim 22, wherein the decoder is
2 further coupled to supply a positive voltage to the
3 deselected wordline if it becomes a selected wordline.

1 24. The system of claim 22, further comprising a
2 second decoder to supply a positive voltage to a selected
3 wordline while the negative voltage is supplied to the
4 deselected wordline.

1 25. The system of claim 22, wherein the decoder
2 comprises a first transistor having a well coupled to
3 receive a negative control voltage, a source terminal
4 coupled to receive the negative voltage, and a drain
5 terminal coupled to pass the negative voltage to the
6 deselected wordline.

1 26. The system of claim 25, further comprising a
2 second transistor coupled to the first transistor and the

3 deselected wordline to pass a program pulse to the
4 deselected wordline if it becomes a selected wordline.

1 27. The system of claim 25, further comprising a pre-
2 driver circuit to disable the first transistor if the
3 deselected wordline becomes a selected wordline.

1 28. The system of claim 22, wherein the memory array
2 comprises a flash memory.

1 29. The system of claim 28, wherein the flash memory
2 comprises a multi-level cell flash memory.

1 30. The system of claim 22, wherein the wireless
2 interface comprises an antenna.